Listing and/or Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A signal processing apparatus, comprising:

[[a]] first and second signal ~~input~~ inputs for receiving ~~an analog signal~~ first and second input signals having [[a]] respective synchronizing ~~characteristic~~ characteristics;

a first clock generator for generating a reference clock signal, the reference clock signal being independent of the synchronizing ~~characteristic~~ characteristics of the ~~analog signal~~ first and second input signals;

a second clock generator, coupled to the first clock generator, for producing a plurality of further clock signals in response to the reference clock signal; and

a signal processing section, coupled to the first and second signal ~~input~~ inputs and the second clock generator, for sampling and processing the ~~analog signal~~ first and second input signals in accordance with a sampling rate and an appropriate signal standard, the signal processing section having a plurality of analog to digital (A/D) converters that are clocked by respective ones of the plurality of further clock signals,

the A/D converters being clocked by respective ones of the plurality of further clock signals, which are independent of the synchronizing ~~characteristic~~ characteristics of the ~~input analog signal~~ first and second input signals and have a frequency substantially equal to the sampling rate, ~~whereby corruption of the analog signal by digital noise in the apparatus is prevented~~ wherein the signal processing section processes the first and second input signals using a single processing channel, the single processing channel being clocked by a further clock signal that has a signal frequency of at least twice the required clocking speed necessary for processing a single one of the first and second input signals.

2. Cancelled.

3. Cancelled.

4. (Currently Amended) The signal processing apparatus of claim [[3]] 1, wherein the ~~analog~~ first and second input signals are television signals.

5. (Previously Presented) The signal processing apparatus of claim 1, wherein the signal processing section is further operable to process a digital input signal having a synchronizing characteristic, and the reference clock signal is independent of the synchronizing characteristic of the digital input signal.

6. (Currently Amended) A television apparatus, comprising:

[[a]] first and second signal ~~input~~ inputs for receiving [[a]] first and second television ~~signal~~ signals having [[a]] respective synchronizing ~~characteristic~~ characteristics;

a first clock signal generator for producing a reference clock signal that is independent of the synchronizing ~~characteristic~~ characteristics of the first and second television ~~signal~~ signals;

a second clock signal generator, coupled to the first clock signal generator, for producing a plurality of further clock signals in response to the reference clock signal;

a signal processor, coupled to the signal ~~input~~ inputs and the second clock signal generator, for sampling and processing the ~~input signal~~ first and second television signals in accordance with [[an]] appropriate signal ~~standard~~ standards and providing [[an]] output ~~signal~~ signals suitable for display on a display device, the signal processor including a plurality of analog to digital (A/D) converters coupled to the second clock signal generator; and

an signal output, coupled to the signal processor, for receiving and coupling the output ~~signal~~ signals to a display device,

the A/D converters of the signal processor being clocked by respective ones of the plurality of further clock signals, which are independent of the synchronizing ~~characteristic~~ characteristics of the input ~~signal~~ signals, and have ~~having~~ a frequency substantially equal to the sampling rate ~~whereby corruption of the analog signal by digital noise in the apparatus is prevented~~, wherein

the signal processing section decodes the first and second television signals using a single processing channel, and the single processing channel is clocked by a clock signal that has frequency of at least twice the required clocking speed necessary for processing a single one of the television signals.

7. Cancelled.

8. Cancelled.

9. (Currently Amended) A method for processing input signals having synchronizing components, the method comprising the steps of:

receiving ~~an input signal~~ first and second input signals having [[a]] respective synchronizing ~~component~~ components;

generating a reference clock signal, the reference clock signal being independent of the synchronizing ~~characteristic~~ characteristics of the ~~input signal~~ first and second input signals;

generating a plurality of further clock signals based on the reference clock signal;

converting the ~~analog input signal~~ first and second input signals into ~~a digital signal~~ corresponding first and second digital signals using analog to digital (A/D) converters that are clocked using one of the plurality of further clock signals; and

decoding the converted digital ~~signal~~ signals in accordance with [[an]] appropriate television signal ~~standard~~ standards using decoding circuitry/logic to provide ~~an output signal~~ output signals suitable for display, the decoding circuitry/logic being clocked by at least one of the plurality of further clock signals, wherein the decoding is performed using a single processing channel that is clocked by an internal clock signal that has a frequency of at least twice the required clocking speed necessary for processing a single input signal

the A/D converters ~~and the decoding circuitry/logic~~ being clocked by respective ones of the plurality of further clock signals, which are independent of the synchronizing characteristic of the input signal and ~~have~~ having a frequency substantially equal to the sampling rate ~~whereby corruption of the analog signal by digital noise is prevented~~.

10. Cancelled.

11. (Previously Presented) The method according to claim 9, wherein

the receiving step further comprises receiving a digital input signal having a synchronizing characteristic, and

the decoding step further comprises decoding the digital input signal using decoding circuitry/logic that is clocked by a respective one of the internal clock signals that is independent of the synchronizing characteristic of the digital input signal.

12. (Previously Presented) The method according to claim 9, wherein

the receiving step comprises receiving an analog television signal.